IN THE CLAIMS:

Please cancel claims 6, 16, and 27 without prejudice or disclaimer, amend claims 1-4, 7-13, 17-24, 26-33 and add claims 34-36 as follows.

1. (Currently Amended) A method for synchronizing a receiver to a transmitter ~~and a receiver~~, comprising ~~the steps of~~:

receiving, by the receiver, a phase difference information indicating a phase difference between an internal clock and an external clock;

~~generating, by the transmitter, phase difference information indicating a phase difference between an internal clock and an external clock;~~

~~transmitting, by the transmitter, the phase difference information to the receiver;~~ ~~and~~

generating, by the receiver, a clock signal dependent on the transmitted phase difference information

generating, by the receiver, an internal clock or recovering an internal clock of the transmitter from information received from the transmitter;

frequency-dividing, by the receiver, the internal clock;

adjusting, by the receiver, the phase of the frequency-divided clock based on the received phase difference information;

storing, by the receiver, at least two successive values of the phase difference information received from the transmitter; and

detecting, by the receiver, a difference between the successive values of phase difference information.~~;~~

2. (Currently Amended) The method according to claim 1, wherein the internal clock and the external clock are frequency-divided ~~clocks~~ within the transmitter to the same frequency, the method further comprising the step of converting the phase difference

between the frequency-divided clocks to a numerical value to be transmitted to the receiver.

3. (Currently Amended) The method according to claim 2, further comprising ~~the step of~~ applying pulses of the frequency-divided clocks to start and stop inputs of a counter which generates the numerical value to be transmitted to the receiver.

4. (Currently Amended) The method according to claim 1, further comprising ~~the step of~~ transmitting the phase difference information to the receiver in the form of multicast packets.

5. (Original) The method according to claim 1, wherein the internal clock is a symbol clock of 80 MHz or 89.6 MHz, and the external clock is an external clock reference of 2.048 MHz or 1.544 MHz.

6. (Cancelled)

7. (Currently Amended) The method according to claim 6, further comprising ~~the step of~~ multiplying, by the receiver, the frequency of the adjusted frequency-divided clock for generating an external clock.

8. (Currently Amended) The method according to claim 7, comprising ~~the step of~~ including, by the receiver, a clock generator stage for generating the external clock, the clock generator stage comprises a first counter for counting, in a round-rotating manner, a high frequency signal, and a second counter for counting the number of rounds of the first counter, the second counter inhibiting the first counter from further counting when reaching a preset value.

9. (Currently Amended) The method according to claim 16, ~~further~~ comprising ~~the steps of~~:

~~storing, by the receiver, at least two successive values of the phase difference information received from the transmitter;~~

~~detecting, by the receiver, a difference between the successive values of phase difference information; and~~

selecting, by the receiver, depending on the difference between the successive values of phase difference information, one of the stored values of the phase difference information for adjusting the phase of the frequency-divided clock.

10. (Currently Amended) The method according to claim 16, ~~further~~ comprising ~~the steps of~~:

~~storing, by the receiver, at least two successive values of the phase difference information received from the transmitter;~~

~~detecting, by the receiver, a difference between the successive values of the phase difference information; and~~

suppressing, by the receiver, depending on the difference between the successive values of the phase difference information, generation of a second pulse within one period of the frequency-divided clock.

11. (Currently Amended) A system for synchronizing a ~~transmitter and a~~ receiver to a transmitter, the system comprises:

a transmitter comprising a phase difference information generating unit configured to generate~~means for generating~~ phase difference information indicating a phase difference between an internal clock and an external clock, and a transmitting unit

configured to transmit~~means for transmitting~~ the phase difference information to the receiver; and

a receiver comprising a receiving unit configured to receive a phase difference information indicating a phase difference between an internal clock and an external clock, a clock generator unit configured to generate~~means for generating~~ a clock signal dependent on the transmitted phase difference information, a generating unit configured to generate an internal clock or recover the internal clock of the transmitter from information received from the transmitter, a frequency-dividing unit configured to frequency-divide the internal clock, an adjusting unit configured to adjust the phase of the frequency-divided clock based on the received phase difference information, a storing unit configured to store at least two successive values of the phase difference information received from the transmitter, and a detecting unit configured to detect a difference between the successive values of phase difference information.~~,~~

12. (Currently Amended) The system according to claim 11, wherein the transmitter further comprises:

a frequency divider ~~means~~unit for frequency dividing the internal clock and the external clock to the same frequency; and

a converting ~~means for converting~~ unit configured to conver the phase difference between the frequency-divided clocks to a numerical value to be transmitted to the receiver.

13. (Currently Amended) The system according to claim 12, wherein the converting ~~means~~ unit comprises a counter which generates the numerical value to be transmitted to the receiver, the counter having start and stop inputs to which pulses of the frequency-divided clocks are applicable.

14. (Original) The system according to claim 11, wherein the phase difference information is transmitted to the receiver in the form of multicast packets.

15. (Original) The system according to claim 11, wherein the internal clock is a symbol clock of 80 MHz or 89.6 MHz, and the external clock is an external clock reference of 2.048 MHz or 1.544 MHz.

16. (Cancelled)

17. (Currently Amended) The system according to claim 16, wherein the receiver further comprises a multiplying ~~means for multiplying~~unit configured to multiply the frequency of the adjusted frequency-divided clock for generating an external clock.

18. (Currently Amended) The system according to claim 17, wherein the receiver further comprises a clock generator stage ~~for generating~~configured to generate an external clock, wherein the clock generator stage comprises a first counter for counting, in a round-rotating manner, a high frequency signal, and a second counter for counting the number of rounds of the first counter, the second counter inhibiting the first counter from further counting when the first counter reaches a preset value.

19. (Currently Amended) The system according to claim 11~~6~~, wherein the receiver further comprises:

~~storages for storing at least two successive values of the phase difference information received from the transmitter;~~

~~a detector means for detecting a difference between the successive values of the phase difference information; and~~

a selector ~~means for selecting~~unit configured to select, depending on the difference between the successive values of the phase difference information, one of the stored values of the phase difference information for adjusting the phase of the frequency-divided clock.

20. (Currently Amended) The system according to claim 16~~1~~, wherein the receiver further comprises:

~~storages for storing at least two successive values of the phase difference information received from the transmitter;~~

~~a detector means for detecting a difference between the successive values of the phase difference information; and~~

a suppressing ~~means for suppressing~~unit configured to suppress, depending on the difference between the successive values of the phase difference information, generation of a second pulse within one period of the frequency-divided clock.

21. (Currently Amended) A transmitter used in a system for synchronizing a ~~transmitter and a~~ receiver to a transmitter, wherein the receiver comprises a clock generator means for generating a clock signal dependent on the transmitted phase difference information, the transmitter comprising:

a plurality of dividers wherein an external synchronization input is applied to one of the plurality of dividers which is configured to generate an external timebase and a symbol clock from an internal clock is applied to another one of the plurality of dividers which is configured to generate an internal timebase of the same frequency as the external timebase

a phase difference generating ~~means for generating~~unit configured to generate phase difference information indicating a phase difference between an internal clock and

an external clock, wherein the internal timebase and the external timebase are applied to start and stop input of the phase difference generating unit;

a symbol generator to which the phase difference is applied, the symbol generator is also configured to receive a symbol clock generated by an internal clock generator; and

a transmitting ~~means for transmitting~~unit configured to transmit the phase difference information to a receiver.

22. (Currently Amended) The transmitter according to claim 21, comprising:

a frequency divider ~~means~~ unit for frequency dividing the internal clock and the external clock to the same frequency; and

a converting ~~means for converting~~unit configured to convert the phase difference between the frequency-divided clocks to a numerical value to be transmitted to the receiver.

23. (Currently Amended) The transmitter according to claim 22, wherein the converting ~~means~~ unit comprises a counter which generates the numerical value to be transmitted to the receiver, the counter having start and stop inputs to which pulses of the frequency-divided clocks are applicable.

24. (Currently Amended) The transmitter according to claim 21, comprising a packet generator ~~means for transmitting~~unit configured to transmit the phase difference information to the receiver in the form of multicast packets.

25. (Original) The transmitter according to claim 21, wherein the internal clock is a symbol clock of 80 MHz or 89.6 MHz, and the external clock is an external clock reference of 2.048 MHz or 1.544 MHz.

26. (Currently Amended) A receiver used in a system for synchronizing a ~~transmitter and a receiver~~receiver to a transmitter, wherein the transmitter comprises a phase difference generating means for generating phase difference information indicating a phase difference between an internal clock and an external clock and means for transmitting the phase difference information to the receiver, the receiver comprising:

a receiving unit configured to receive a phase difference information indicating a phase difference between an internal clock and an external clock;

a clock generator unit configured to generate~~means for generating~~ a clock signal dependent on a phase difference information transmitted from a transmitter;

a generating unit configured to generate an internal clock, or to recover the internal clock of the transmitter from information received from the transmitter;

a frequency-dividing unit configured to frequency-divide the internal clock;

an adjusting unit configured to adjust the phase of the frequency-divided clock based on the received phase difference information;

storages for storing at least two successive values of the phase difference information received from the transmitter; and

a detector unit configured to detect a difference between the successive values of the phase difference information.

27. (Cancelled)

28. (Currently Amended) The receiver according to claim 26, further comprising a multiplying ~~means for multiplying~~unit configured to multiply the frequency of the adjusted frequency-divided clock for generating an external clock.

29. (Currently Amended) The receiver according to claim 26, further comprising a clock generator stage ~~for generating~~configured to generate an external clock, the clock generator stage comprises a first counter for counting, in a round-rotating manner, a high frequency signal, and a second counter for counting the number of rounds of the first counter, the second counter inhibits the first counter from further counting when the first counter reaches a preset value.

30. (Currently Amended) The receiver according to claim 26, comprising:

~~storages for storing at least two successive values of the phase difference information received from the transmitter;~~

~~a detector means for detecting a difference between the successive values of the phase difference information; and~~

a selector ~~means for selecting~~unit configured to select, depending on the difference between the successive values of the phase difference information, one of the stored values of the phase difference information for adjusting the phase of the frequency-divided clock.

31. (Currently Amended) The receiver according to claim 26, comprising:

~~storages for storing at least two successive values of the phase difference information received from the transmitter;~~

~~a detector means for detecting a difference between the successive values of the phase difference information; and~~

a suppressing unit configured to suppress~~means for suppressing~~, depending on the difference between the successive values of the phase difference information, generation of a second pulse within one period of the frequency-divided clock.

32. (Currently Amended) A method for synchronizing a ~~transmitter and a~~ receiver to a transmitter wherein the receiver generates a clock signal dependent on a transmitted phase difference information, the method comprising ~~the steps of~~:

applying an external synchronization input to one of a plurality of dividers which is configured to generate an external timebase and applying a symbol clock from an internal clock to another one of the plurality of dividers which is configured to generate an internal timebase of the same frequency as the external timebase;

generating, by a transmitter, phase difference information indicating a phase difference between an internal clock and an external clock, wherein the internal timebase and the external timebase are applied to start and stop input of the phase difference generating unit;

applying the phase difference to a symbol generator, the symbol generator is also configured to receive a symbol clock generated by an internal clock generator; and

transmitting, by the transmitter, the phase difference information to the receiver.

33. (Currently Amended) A method for synchronizing a ~~transmitter and a~~ receiver to a transmitter wherein the transmitter generates phase difference information indicating a phase difference between an internal clock and an external clock, the method comprising ~~the step of~~:

receiving, by the receiver, a phase difference information indicating a phase difference between an internal clock and an external clock;

generating, by the receiver, a clock signal dependent on a transmitted phase difference information indicating a phase difference between the internal and the external clock of the transmitter, the phase difference information being received from the transmitter;

generating, by the receiver, an internal clock or recovering the internal clock of the transmitter from information received from the transmitter;

frequency-dividing, by the receiver, the internal clock;

adjusting, by the receiver, the phase of the frequency-divided clock based on the received phase difference information;

storing, by the receiver, at least two successive values of the phase difference information received from the transmitter; and

detecting, by the receiver, a difference between the successive values of phase difference information.

34. (New) A system for synchronizing a transmitter and a receiver, the system comprising:

a transmitter comprising a phase difference information generating means for generating phase difference information indicating a phase difference between an internal clock and an external clock, and transmitting means for transmitting the phase difference information to the receiver; and

a receiver comprising a receiving means for receiving a phase difference information indicating a phase difference between an internal clock and an external clock, a clock generator means for generating a clock signal dependent on the transmitted phase difference information, generating means for generating an internal clock or recovering the internal clock of the transmitter from information received from the transmitter, frequency-dividing means for frequency dividing the internal clock, adjusting means for adjusting the phase of the frequency-divided clock based on the received phase difference information, storing means for storing at least two successive values of the phase difference information received from the transmitter, and detecting means for detecting a difference between the successive values of phase difference information.

35. (New) A transmitter used in a system for synchronizing a transmitter and a receiver, wherein the receiver comprises a clock generator means for generating a clock signal dependent on the transmitted phase difference information, the transmitter comprising:

applying means for applying an external synchronization input to one of a plurality of dividers which is configured to generate an external timebase and applying a symbol clock from an internal clock to another one of the plurality of dividers which is configured to generate an internal timebase of the same frequency as the external timebase;

a phase difference generating means for generating phase difference information indicating a phase difference between an internal clock and an external clock, wherein the internal timebase and the external timebase are applied to start and stop input of the phase difference generating means;

applying means for applying the phase difference to a symbol generator, the symbol generator is also configured to receive a symbol clock generated by an internal clock generator; and

a transmitting means for transmitting the phase difference information to a receiver.

36. (New) A receiver used in a system for synchronizing a transmitter and a receiver, wherein the transmitter comprises a phase difference generating means for generating phase difference information indicating a phase difference between an internal clock and an external clock and means for transmitting the phase difference information to the receiver, the receiver comprising:

a receiving means for receiving a phase difference information indicating a phase difference between an internal clock and an external clock;

a clock generator means for generating a clock signal dependent on the transmitted phase difference information;

generating means for generating an internal clock or recovering the internal clock of the transmitter from information received from the transmitter;

frequency-dividing means for frequency dividing the internal clock, adjusting means for adjusting the phase of the frequency-divided clock based on the received phase difference information;

storing means for storing at least two successive values of the phase difference information received from the transmitter; and

detecting means for detecting a difference between the successive values of phase difference information.